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Quarterly Progress Report

(January 1, 1992 through March 31, 1992)

on

VLSI for High-Speed Digital Signal Processing

prepared for

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We have continued our development of the 12-bit by 11-bit multiplier for our multiprocessor-ring chip. Since the multiplier's performance is the single most important factor in determining the maximum speed at which our system can operate, it is essential that this task be performed in the best possible manner. Our goal was that this multiplier operate in approximately 30 ns, so that our overall chip speed could reach 30 MHz. The multiplier was designed to accommodate eleven-bit data and twelve-bit coefficients. In addition to the above-cited operating speed goal, we needed to make the multiplier small enough that five complete processors, including five multipliers, can be included on a single IC (which employs 2-μm CMOS technology). As mentioned in the previous progress report, after completing the multiplier's layout and verifying its correct functioning via logic simulation, we performed SPICE simulations on the various multiplier critical-path components. These simulations indicated an operating speed well under 30 ns. We next fabricated a MOSIS TinyChip (2.22 mm $\times$ 2.25 mm, in 2-μm technology) with this 12-bit by 11-bit multiplier and a small block of coefficient RAM as well as a small dual-port register block. This allowed us to test the multiplier's performance in an environment that closely simulates the five-processor-ring system.

During the present quarter the fabricated TinyChip was tested using the Tektronix LV500 logic verification system, and the results verified the multiplier's proper

functioning. The overall delay of the TinyChip was measured to be 36 ns. The critical path of the multiplier is therefore approximately 26 ns (subtracting off the read time of the dual-port RAM — approximately 10 ns). This is well below the 30 ns goal and corresponds well to the expected (simulation) result of 26.4 ns. Furthermore, while this design was being fabricated, we laid out a redesigned vector-merge portion of the multiplier. The simulated critical path of the new design is 22.3 ns. Since the multiplier determines the operating speed of the overall five-processor ring chip, we now expect the completed project to operate at approximately 40 MHz, far exceeding the proposed 30 MHz goal, and a quite good performance level in absolute terms, considering the small size of our multipliers, and considering that they are fabricated using 2-μm CMOS technology. Another MOSIS TinyChip will be sent out for fabrication this quarter which employs the multiplier with the re-designed vector-merge block.

We have also begun the IC layout of the storage registers for the program instructions used by our processors. We expect this layout to be completed during the present quarter. Furthermore, work has been proceeding nicely on the IC layout of the ALU. This has been approached by starting with the layout of the multiplier and gradually extending it according to the specified ALU architecture.

Another project has been started during the present quarter. It concerns a novel signed-digit serial multiplier, which should prove useful for new real-time FFT and adaptive-filtering applications.

Two journal publications citing ONR support under this grant have appeared during the present quarter:

(1) B-R. Horng, H. Samueli, and A. N. Willson, Jr., "The Design of Low-Complexity Linear-Phase FIR Filter Banks Using Powers-of-Two Coefficients with an Application to Subband Image Coding," *IEEE Trans. on Circuits and Systems for Video Technology*, vol. 1, December 1991, pp. 318-324.

(2) B-R. Horng and A. N. Willson, Jr., "Lagrange Multiplier Approaches to the Design of Two-Channel Perfect-Reconstruction Linear-Phase FIR Filter Banks," *IEEE Trans. on Signal Processing*, vol. 40, February 1992, pp. 364-374.

In addition, our paper describing the multiprocessor–ring has been accepted for the June 1992 special issue of the *IEEE Trans. on Circuits and Systems for Video Technology*, and a shortened version of this paper has been accepted for the U.R.S.I. International Symposium on Signals, Systems and Electronics, in Paris, September 1-4, 1992. Copies of these papers and acceptance notices are enclosed. Finally, we have received notice that our neural network paper (submitted with last quarter's progress report) has been accepted by the IJCNN '92 conference in Baltimore. A copy of that acceptance letter is also enclosed.

Statement A per telecon
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